Supplementary Information for Graphene-Sealed Flow Cells for *In Situ* Transmission Electron Microscopy of Liquid Samples

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The fabrication process for the GFC is illustrated schematically in Table 1. For concreteness we describe here the fabrication and testing of GFCs in which the top window is graphene and the bottom window is very thin Si_3N_4. We utilize two versions of the nanochannel chip, the first with Si_3N_4:SiO_2: Si_3N_4 = 25nm:100nm:25nm, and the second with Si_3N_4:SiO_2: Si_3N_4 = 14nm:70nm:7nm. These stacks are deposited onto a 300μm thick 4-inch silicon wafer (100). We pattern the gold electrode using the lift-off technique. Next, we open a window on the backside of the wafer using a plasma etch. This opens up the SiN/ SiO_2/SiN stack, exposing the silicon underneath. We perform a KOH etch until the silicon is completely consumed and the Si_3N_4 layer is revealed. Next, we pattern channels in the Si_3N_4:SiO_2: Si_3N_4. To do this, the channel chip is first spin-coated with two layers of PMMA. We then use electron beam (ebeam) patterning to create an array of individual point exposures spaced 1μm apart which define the eventual locations for holes in the top Si_3N_4 layer. We then create these holes using an SF_6 plasma etch. The continuous nanochannel under the array of holes is fomed using a wet buffered hydrofluoric acid (BHF) etch, which removes SiO_2 from beneath each hole, leaving a hollow cylindrical chamber in the SiO_2. As etching continues, the cylindrical chambers or cavities become interconnected, leading to a continuous channel with headroom between the perforated upper Si_3N_4 layer and the continuous Si_3N_4 layer spaced 70nm or 100nm below it.

Monolayer graphene is produced using well-established methods.[1] For multi-layer graphene, we coil copper foil inside a 1-inch diameter quartz tube and anneal it under 200sccm H_2 in vacuum at 1025°C for 1hr. We then close the vacuum valve and allow the tube to pressurize to 1atm before opening the exhaust valve. 18sccm CH_4 is then introduced in addition to the 200sccm H_2 for a 1hr growth time. We confirm the graphene thickness to be monolayer or few-layer using Raman spectroscopy, then spin-coat this graphene with PMMA and etch away the copper substrate using a sodium persulphate solution. We wet-transfer the floating PMMA/graphene bilayer onto the channel chip, and subsequently remove the PMMA using either acetone or an annealing process.

The graphene-windowed nanochannel chip described above is mated to a complementary smaller second chip: the top plate. The top plate provides the interface to an external fluid source and drain piping. It is fabricated with a slit and its own fluidic channels. Fabrication steps are shown in table 2. To ensure a leak-free seal when the nanochannel chip and top plate are mated, metals are evaporated onto the bonding surface of each chip to create a soft metal gasket. Using electron beam evaporation, we sequentially add 1nm of Cr, 10nm of Au, and 5μm of indium onto the top plate; and 1nm of Cr and 10nm of Au onto the nanochannel chip. The two chips are then press-fit together inside a custom chuck that is a replica of the Poseidon flow cell holder where they will eventually be placed. To bond the two chips together, the force-loaded chuck is heated to 200°C for approximately 30s before being slowly cooled to room temperature. This assembly process in described in table 3.

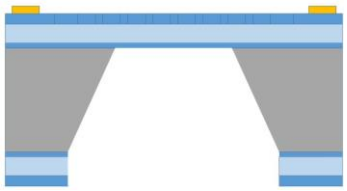
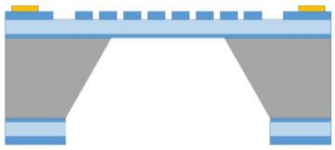
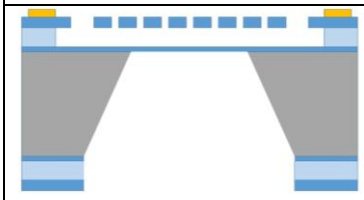
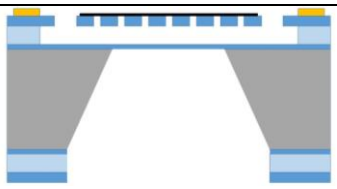
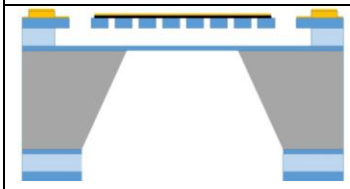
	300μm thick, double-side polished, 4” Si wafers are used for batch fabrication of nanochannel chips.
	A stack of $Si_3N_4/SiO_2/Si_3N_4$ is deposited by LPCVD to each side of the wafer.
	Metal contacts (Au/Cr) serving as alignment markers are patterned and deposited on the top of the chip.
	A suspended $Si_3N_4/SiO_2/Si_3N_4$ stack is produced (released) by a backside KOH etch after opening up silicon on the backside with RIE etch.
	The nanochannel is patterned by ebeam point exposures in PMMA followed by a RIE of the top Si_3N_4 layer. This is followed by PMMA strip.
	The sandwiched SiO_2 is selectively etched away using a BHF etch, creating a row of interconnected cylindrical cavities which form the nanochannel. The nanochannel, running left to right, will be formed within the suspended stack.
	Graphene is deposited over the holes in the Si_3N_4 covering the top of the nanochannel. The bottom of the nanochannel remains thin Si_3N_4.
	A thin layer of gold (10 nm) is deposited on top of the channel as an Indium bonding promoter.

Table 1: Fabrication steps for Nano channel chip (Bottom chip). Grey is silicon. Blue is Si_3N_4. Light blue is SiO_2. Yellow is gold.

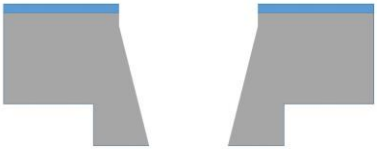
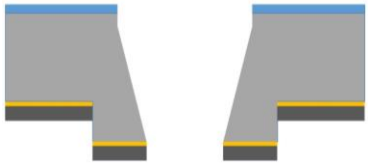
	300µm thick, double-side polished, 4” Si wafers are used for batch fabrication of top chips.
	Microfluidic channel is etched into silicon using DRIE (10-20µm deep).
	Si_3N_4 is deposited by LPCVD to each side of the wafer.
	A window is opened up in the silicon nitride using RIE exposing underlying Silicon.
	KOH etch is used to etch away silicon, leaving a SiN membrane.
	Nitride membrane is etched away from the front side using CF_4/CHF_3 etch.
	10nm layer of gold followed by 2-4µm layer of indium are deposited by ebeam evaporator.

Table 2: Fabrication steps for the top chip. Grey is silicon. Blue is Si_3N_4. Yellow is gold. Dark grey is indium.

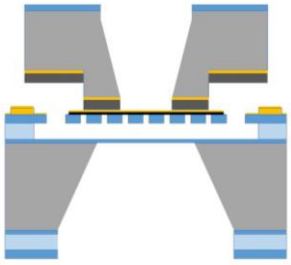
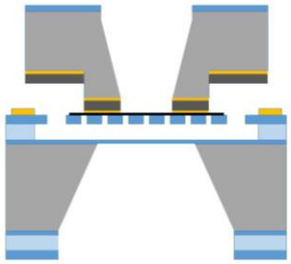
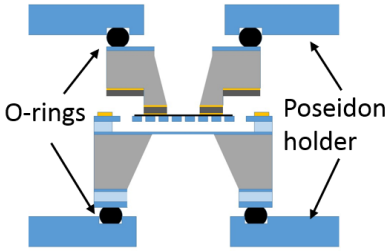
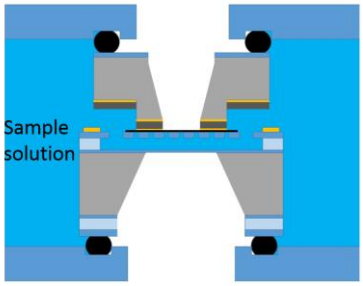
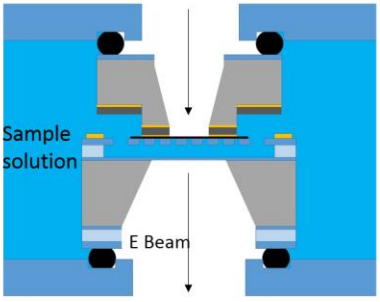
	The two chips are then press-fit together inside a custom chuck. The force-loaded chuck is heated to 200°C for approximately 30s before being slowly cooled to room temperature.
	After bonding, excess Au is etched from the exposed region of the nanochannel using an iodine-based wet etchant by dropping the etching solution in the KOH pocket of the top chip. This is followed by DI water rinse and IPA dry.
	This full assembly fits into Protochips Poseidon TEM holder with supplied O-rings.
	Inject the sample using the syringe pump with the required solution. Leak check can be done before inserting into the TEM.
	TEM imaging is done at 80 KeV

Table 3: Final assembly of the chips and TEM holder. Grey is silicon. Blue is Si3N4. Yellow is gold. Dark grey is Indium.

This full assembly is compatible with Protochips Poseidon TEM holder. We introduce DI water into the TEM holder for optical imaging using a custom built set up (Figure 4) and leak check the channel before introduction to the high vacuum TEM environment. Then we introduce the sample solution just before loading into the TEM.

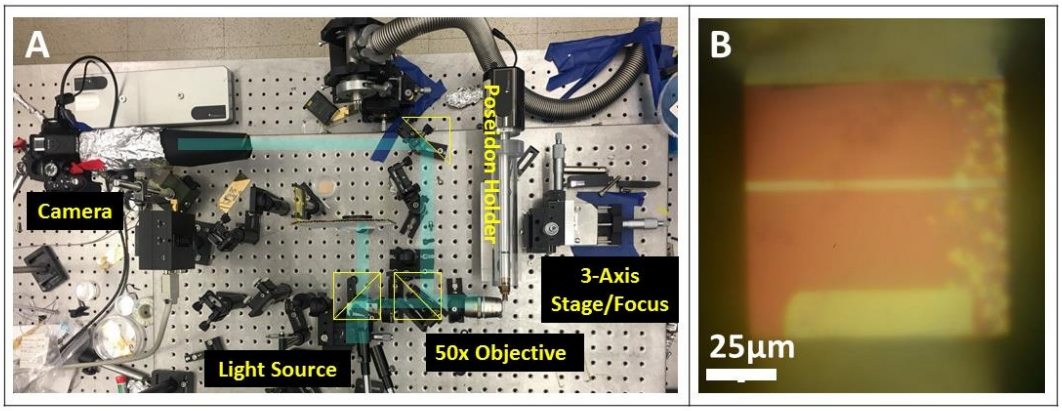


Figure 4: Optics used to image flow cell during introduction of the liquid into GFC.

References:

(1) Li, X.; Cai, W.; An, J.; Kim, S.; Nah, J.; Yang, D.; Piner, R.; Velamakanni, A.; Jung, I.; Tutuc, E.; Sanjay K. Banerjee, Luigi Colombo, Rodney S. Ruoff, Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils. *Science* **2009**, *324*, 1312–1314.